class A and the last two push-pull stages class B. The typical midband gain is 40dB. Since collector to base feedback is used only input and output waveforms are truly meaningful. However, collector waveforms on each pair should appear balanced. Normally transistors should be replaced in pairs.

Due to the high current drawn by the amplifier (up to 20 amps) collector voltage is present at all times. Therefore even with the set turned off a small leakage current flows (15-20 ma typical). Grounding the PTT line turns Q6 on and applies bias to all stages.

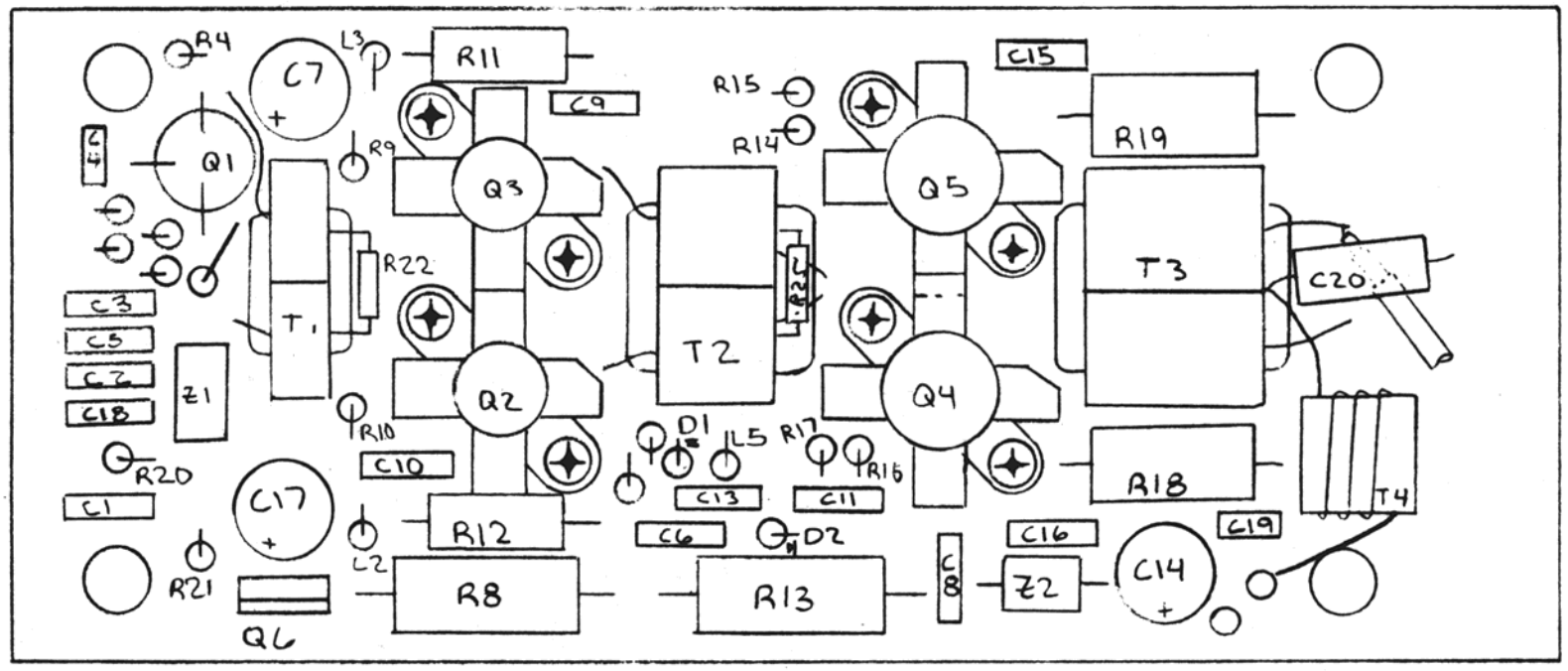
## 16.0 RF TUNING ASSEMBLY

The RF tuning assembly contains three sets of filters controlled by the band switch. One set of bandpass filters for transmit, and one set for receiver, plus the transmit output lowpass filters. The 5 element 10M lowpass filter is always inline. In addition to the filters the assembly also contains the T-R relay and voltage switching to indicate the band for other circuits.

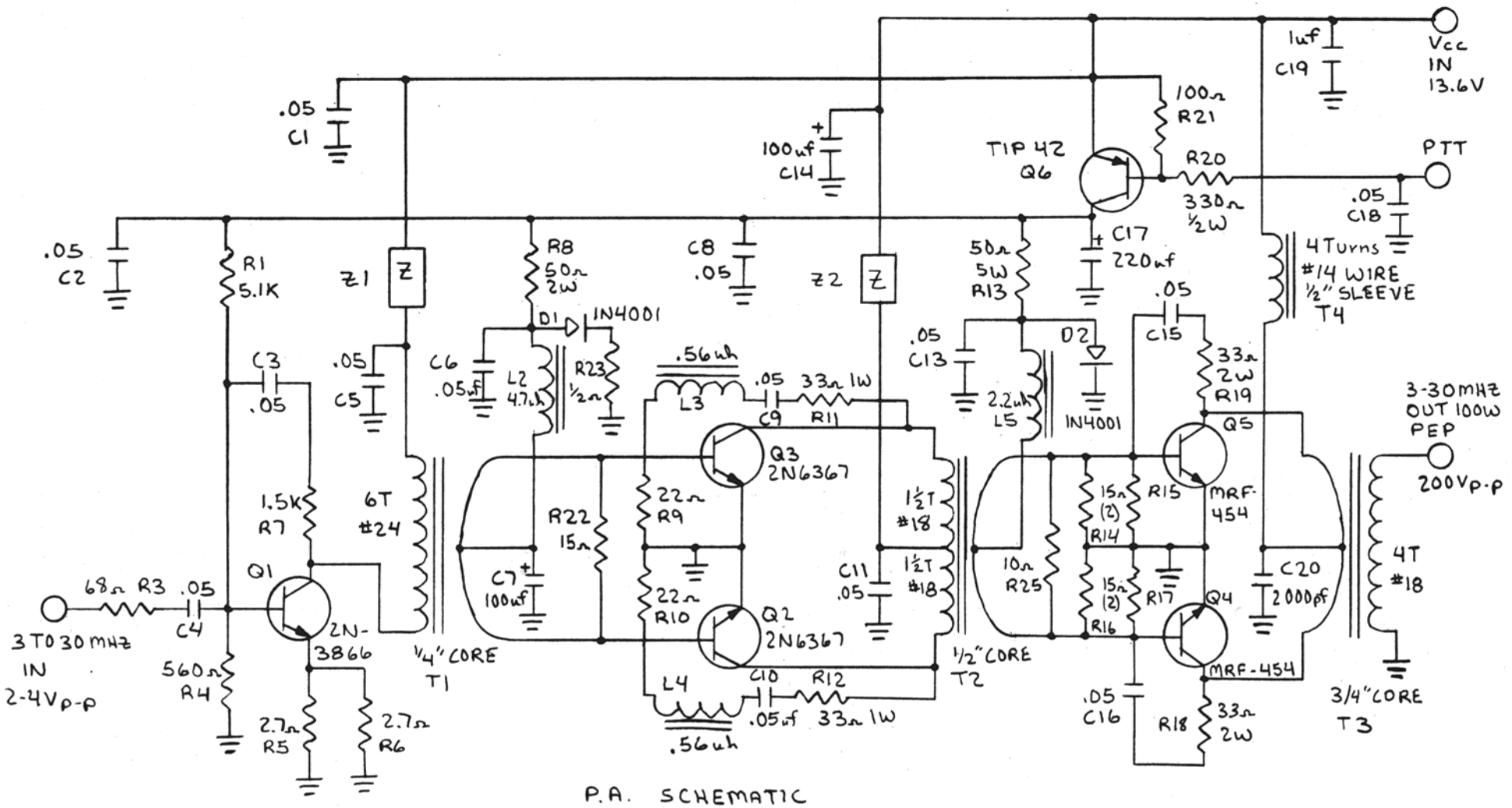
Alignment: Filter coils should be tuned to center filter response in the bands as listed below:

1. Receiver

| Band | L numbers | Frequency MHz |
|---|---|---|
| 80 | 101,102 | 3.5 - 4.5 |
| 40 | 103,104 | 7.0 - 7.5 |
| 20 | 105,106 | 14.0 -14.5 |
| 15 | 107,108 | 21.0 -21.5 |
| 10 | 109,110 | 28.0 -30.0 |
| WWV | 111 | 10.0 |

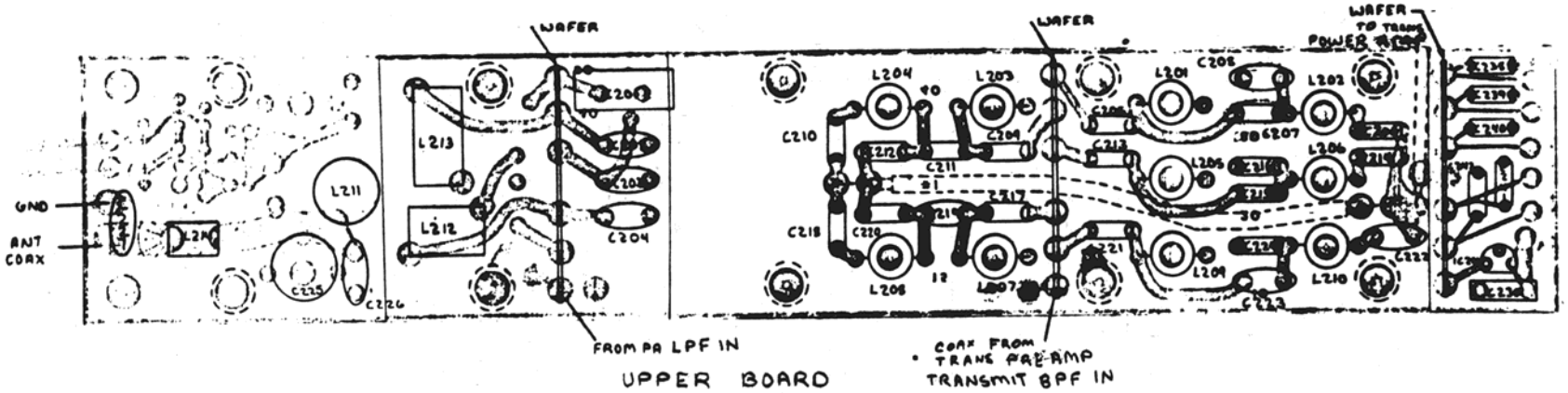

R4
C7
L3
R11
C9
R15
R14
C15
R19
Q1
R9
Q3
Q5
T3
C20
R22
T1
T2
C3
C5
C7
C18
Z1
Q2
Q4
R10
D1
L5
R17
R16
C10
C13
C11
R18
T4
R20
C1
C17
R12
C6
D2
C16
C19
R21
L2
R8
R13
C8
Z2
C14
Q6

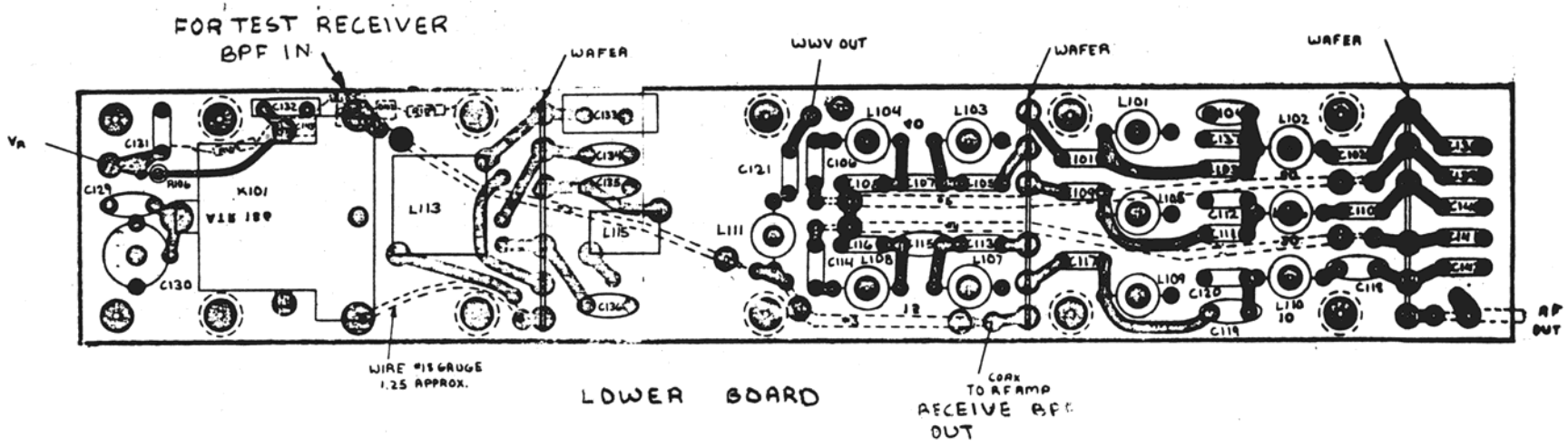
LAYOUT 15



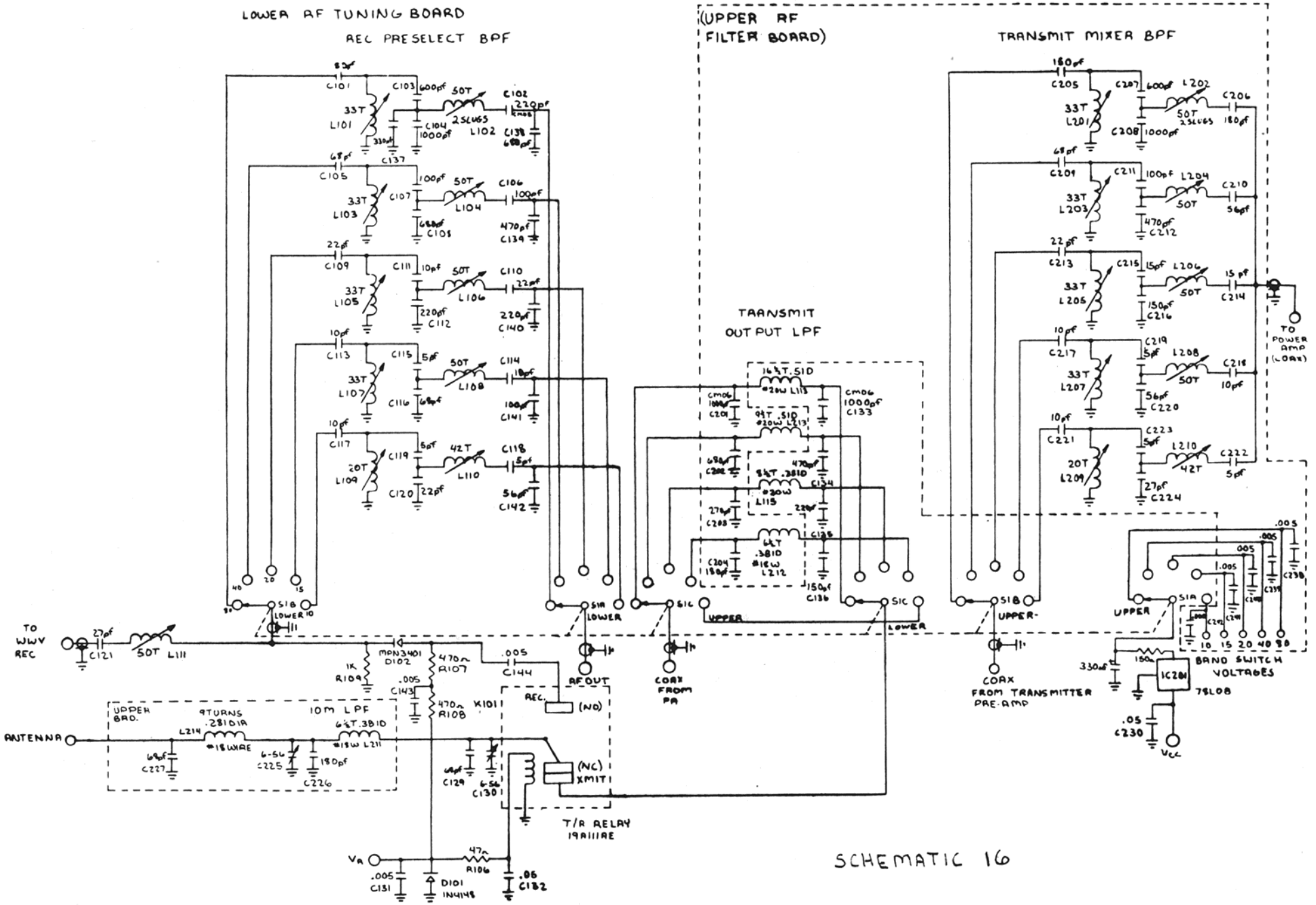

P.A. SCHEMATIC

SCHEMATIC 15


WAFER
WAFER
WAFER
TO TRANS
POWER
GND
ANT
COAX
L211
L213
L212
C225
C226
C204
L204
L203
L201
C205
L202
C210
C211
C213
C218
C219
C217
L205
L206
L209
L210
C221
C222
FROM PA LPF IN
COAX FROM
TRANS PRE-AMP
TRANSMIT BPF IN
UPPER BOARD


FOR TEST RECEIVER
BPF IN
WAFER
WWV OUT
WAFER
WAFER
VA
C131
C129
C130
K101
L113
L115
L104
L103
L101
L102
C121
C111
L111
L108
L107
L109
C120
C119
L110
AF
OUT
WIRE #18 GAUGE
1.25 APPROX.
COAX
TO RF AMP
RECEIVE BPF
OUT
LOWER BOARD

LAYOUT 16


LOWER RF TUNING BOARD
REC PRESELECT BPF
(UPPER RF FILTER BOARD)
TRANSMIT MIXER BPF
TRANSMIT OUTPUT LPF
TO WWV REC
ANTENNA
10M LPF
UPPER BRD.
9TURNS .2810IA #18WIRE L214
6&T.3810 #18W L211
REC.
(NO)
(NC) XMIT
T/R RELAY 19A111RE
K101
AF OUT
COAX FROM PA
COAX FROM TRANSMITTER PRE-AMP
UPPER
LOWER
TO POWER AMP (COAX)
BAND SWITCH VOLTAGES
IC204
7805B
Vcc
VR
D101 1N4148
MPN3401 D102
D103
SCHEMATIC 16

2. Transmit

| Band | L numbers | Frequency MHz |
|---|---|---|
| 80 | 201,202 | 3.5 - 4.5 |
| 40 | 203,204 | 7.0 - 7.5 |
| 20 | 205,206 | 14.0 - 14.5 |
| 15 | 207,208 | 21.0 - 21.5 |
| 10 | 209,210 | 28.0 - 30.0 |

3. Transmit: Fixed elements

## 17.0 VOLTAGE REGULATORS AND NEGATIVE POWER SUPPLY

The transmitter power amplifier, audio power amplifier, and readout bright voltage are all unregulated input voltage. All other circuits operate from multiple regulated voltages. On synth #2 circuit board is the system 11V regulator. This feedback type regulator can operate with input supply voltages as low as 11.7 VDC and still hold regulation. The 8V regulator IC23 is used as the reference for regulator feedback amplifier IC25. Transistor Q6 and the chassis mounted TIP-42 form the active pass network. Diodes D23 and D4 are a start up network. All circuits in the unit (except those mentioned above) are supplied by this 11V regulator. In most cases the circuits operate on 8VDC supplied by local on board regulators or 5VDC supplied by chassis mounted regulators.

To supply the required negative supply voltage for some operational amplifiers a TTL divider signal is used to drive a buffer switch (Q28) on the synth. #2 board. The buffer output is AC coupled and rectified to give an output of about -5VDC.

## 18.0 DIGITAL SYNTHESIZER GENERAL DISCUSSION

In general the digital synthesizer can be broken down to 6 basic components:

A. Major Loop
The major loop VCO output operates at the desired LO frequency. The VCO operates at N 100Hz where N is programmable divider number.

B. Minor Loop
The minor loop output is mixed with the major loop output to give a constant frequency input to the programmable divider. This allows the same values of N for all bands. In addition the minor loop frequency is altered to correct for sideband selected.

C. Up/Down Counter
This counter is clocked up or down by the tuning switches to alter the program in the programmable counter and hence the LO frequency.

D. Bandedge Decoder
Bandedge decoding is done by comparing the programming number with an allowed number set. If the programming number is out of preset bounds the up/down counter is reset to the nearest band edge.

E. Reference Generator
The basic frequency standard for the entire system is

a 5MHz crystal oscillator. This oscillator is used in three ways:

a. LO for WWV receiver

b. Divided by $5x10^4$ to generate 100Hz reference for major loop.

c. Divided by $3.03x10^4$ to generate 165.0165Hz reference for minor loop.

F. Readout

The status of the program number is adjusted to match frequency and fed to an LED multiplexing system. (See table 1).

## 19.0 DIGITAL SYNTHESIZER DETAILED DISCUSSION

In this section each of the major components are described in detail. Exact frequencies and divider numbers for each band are listed in table 1.

A. Major Loop

Circuits discussed herein are on Synth #2 circuit board unless noted otherwise.

The major loop VCO is a 5 band LC oscillator (Q22) with each band selected by switching on the desired transistor switch (Q18 through Q21). Frequency change is by control voltage applied to R141 to control the capacity of C95; a varicap diode. Bias voltage for the varicap and oscillator transistor is double regulated by D6 and IC27. VCO output is buffered and isolated by transistors Q23 through Q26. One buffered output is the transceiver L.O. and the other drives

one input of the synthesizer mixer.

The mixer output drives the programmable divider to generate the "data" input to the frequency/phase detector, IC19. The data input is coupled to pin 1 of IC19, but due to the high divider number the TTL pulse is very difficult to see on a scope. Its presence can be inferred by pulse waveforms on pins 13 or 10. The 100Hz data pulse may also be checked with a counter. Pin 8 is the semi-filtered DC correction voltage. IC21 is a notch filter to remove 100Hz components from the correction voltage. This notch filter is followed by a passive RC filter network which feeds R141.

The programmable divider is on the Synth #1 circuit board and consists of IC's 21 through 25. The divider reset pulse and the data output pulse is generated by a oneshot multivibrator 1/2 IC8. Input frequency range to the divider is 2-4MHz.

Major loop alignment: VCO adjustment must be made in sequence 10M, 15M, 20M, 40M, and 80M. Adjustments should be made with each band at the lowest frequency in each band. Tune each coil for a correction voltage of 2.5V $\pm$ .25V measured on R18. For units that tune 27MHz the correction voltage on 10M is set to 3.0VDC. To adjust the notch filter set R11 and R15 for minimum amplitude waveform as shown on schematic.

B. Minor Loop

All circuits of minor loop are on Synth #2 circuit board. The minor loop VCO operation is similar to

The major loop VCO. The output of buffer, Q8, drives the second input of the synthesizer mixer. The mixer output is the difference of the two VCO inputs.

The buffer output is a TTL compatible clock to drive a high speed divide by 10 prescaler, IC16. The output of IC16 is approximately .7 to 3.15MHz depending on band and sideband selected. This output drives a 5 stage counter, IC11 through 15. This counter uses a similar reset and data output one-shot MV, 1/2 IC10. Program for the divider is derived from two 32 x 8 PROMS, IC's 17 and 18. The sideband and operating band are the inputs to generate correct program code.

Frequency/phase detector, notch filter (tuned to 165 Hz), and RC filter operation are similar to the major loop.

Minor loop alignment: As with the major loop the VCO must be aligned in order 10M through 80M. The correction voltage on each band should be set to 1.6V $\pm$ .2VDC as measured on R21. To adjust the VCO it is necessary to remove the brass shield by unsoldering the three corners. To adjust the notch filter set R25 and R27 for minimum amplitude waveform as shown on schematic. This waveform will vary somewhat in size and shape depending on band.

C. Up-Down Counter

This circuit is on the Synth #1 circuit board. The

up-down counter is a 5 stage ripple counter with BCD outputs on each stage to program corresponding stages of the major loop divider. IC's 16 through 20 comprise this divider.

Clocking of this divider is done by gating the output of a multivibrator 1/4 IC32 through an up or down gate to the correct input of the counter. These up or down gates associated with the oneshot MV, 1/2 IC31 form a debounce circuit and a slight start delay to permit single steping the synthesizer. The rate is varied by the time constant capacitor selected.

The BCD program numbers available are limited by the bandedge decoder which resets the up-down counter at preset limits.

No adjustment or alignment is necessary.

D. Bandedge Decoder

Bandedge decoding is done by checking the program of the two most significant digits of the major loop divider. A greater-than or less-than comparison is done by IC's 6 and 7. These magnitude comparitors alternately look for divider numbers greater than upper limits or lower than lower than lower limits. If an out of bounds condition is found the up-down counter is reset and a correct number is preset in the counter. A series of gates and oneshot MV's are used for timing, and program resets for the up-down counter.

E. Reference Generator

The reference oscillator and its associated dividers are located on Synth #2 circuit board.

Basic frequency reference for the transceiver is derived from a 5MHz crystal oscillator. This oscillator drives a pair of divider chains to generate 100Hz TTL for the major loop and 165Hz TTL for the minor loop. IC's 4 and 5 divide the 5MHz by 100. For the major loop IC's 1 through 3 divide the output of IC4 by 500 to generate the 100Hz TTL reference for the major loop. For the minor loop IC's 6 through 8 divide the output of IC4 by 303 to generate the 165Hz reference for the minor loop. The divide by 303 circuit is similar to the other ripple counters in the synthesizer in that it uses a oneshot MV to generate the divider reset and the reference pulse to the minor loop frequency/phase detector.

The 5MHz output is also used to provide the drive to the WWV receiver L.O. multiplier.

F. Readout Circuits

All readout circuits are located on Synth #1 circuit board. Information regarding band and divider number is fed to PROMS, IC1 and IC30, and to the multiplex buffers IC's 10 through 15.

Basic function is as follows: A Schmitt trigger gate is used as a multiplex clock oscillator. This oscillator drives a BCD counter (IC26) which in turn drives

a BCD to decimal decoder (IC27). The decoded outputs are used to drive digit enable circuits, and the multiplex buffers. The multiplexed digit data is fed to a BCD to 7 segment decoder (IC29).

| BAND | FREQ | S.B. | 1st L.O. | SYNTH L.O. | SYNTH MIXER MHz | N REF= 100Hz | M REF= 165.0165Hz |
|---|---|---|---|---|---|---|---|
| | 3.5 | USB | 9.10165 | 7.00165 | 2.1000 | 21000 | 42430 |
| | | LSB | 9.09835 | 6.99835 | | | 42410 |
| 80M | | | | | | | |
| | 4.0 | USB | 9.60165 | | 2.6000 | 26000 | |
| | | LSB | 9.59835 | | | | |
| | 7.0 | USB | 12.60165 | 10.50165 | 2.1000 | 21000 | 63640 |
| | | LSB | 12.59835 | 10.49835 | | | 63620 |
| 40M | | | | | | | |
| | 7.5 | USB | 13.10165 | | 2.6000 | 26000 | |
| | | LSB | 13.09835 | | | | |
| | 14.0 | USB | 19.60165 | 17.50165 | 2.1000 | 21000 | 106060 |
| | | LSB | 19.59835 | 17.49835 | | | 106040 |
| 20M | | | | | | | |
| | 14.5 | USB | 20.10165 | | 2.6000 | 26000 | |
| | | LSB | 20.09835 | | | | |
| | 21.0 | USB | 26.60165 | 24.50165 | 2.1000 | 21000 | 148480 |
| | | LSB | 26.59835 | 24.49835 | | | 148460 |
| 15M | | | | | | | |
| | 21.5 | USB | 27.10165 | | 2.6000 | 26000 | |
| | | LSB | 27.09835 | | | | |
| | 28.0 | USB | 33.60165 | 31.50165 | 2.1000 | 21000 | 190900 |
| | | LSB | 33.59835 | 31.49835 | | | 190880 |
| 10M | | | | | | | |
| | 29.999 | USB | 35.60065 | | 4.0990 | 40990 | |
| | | LSB | 35.59735 | | | | |

TABLE 1

TROUBLE SHOOTING GUIDE

Most frequent problems & causes.

Transmitter:

| Symptom | Possible Cause | Remarks |
|---|---|---|
| No power out (or low power out) | No DC power to P.A. | ---------- |
| | No drive to P.A. | In CW mode check output of transmit preamp to determine if fault is in drive or P.A. If drive ok see below. If no drive trace $f_{CX}$ & LO circuits to determine fault. |
| | Power Amplifier failure | If maximum power output is 1-10 Watts the cause is usually burned out final transistors. If power output is about 50 watts usually 1 of the final pair is blown. The final transistors should always be replaced in pairs. If finals are blown this is usually caused by overheating of heatsink. Either due to excessive power output or lack of cooling air. |
| | Driver Transistor failure | Driver failure is unusual & symptoms are similar to final problems. Ohmic or signal tracing tests can be used to determine failed devices. Note: The power amplifier may be operated opened away from main chassis but care must be used to prevent shorting and overheating. |

| | | |
|---|---|---|
| | Reverse or Over Voltage | Since the PA is connected directly to the Vcc bus, over or reverse voltage will destroy all r transistors in the PA. Damage to other circuits in set is minimal. For operation where reverse connection is likely an available diode protected & fused cable should be used. |
| | T-R Relay | Since the antenna is connected to the transmitter through the normally closed contacts of the relay this failure mode is unusal. If a problem occurs it can usually be corrected by cleaning contacts with WD-40. The contacts are available through a .5 inch hole in the bottom of the RF assembly. |

Receiver:

| Symptom | Possible Cause | Remarks |
|---|---|---|
| No noise or received signal. | | |
| | No Vr | Check for Vr on R63. |
| | No Supply Voltage | Check for 8V at outputs of 8V IC voltage regulators IC's 1 and 4. |
| | No Carrier Oscillator | Change modes USB to LSB for example to determine if oscillator is functional on other modes. Oscillator output is available on R268. |

| | |
|---|---|
| No audio output | Noise or audio present at R284? Yes: Check signal path to audio PA through volume control. No: Check signal path through receiver. |
| Reduced Threshold 10 to 40dB | |
| T-R Relay | Check voltage to relay coil at bottom rear of RF assembly. In receive mode is voltage about 12VDC? No: Check relay driver Q51. Yes: Check for relay pull in. Observe through .5 inch hole in bottom of RF assembly. Note proper seating of contacts & complete pull in of coil. Clean contacts with WD-40. |
| RF Amp. | Is RF amp gain 10dB? Measure gain from cable input to emitter of Q2 using low-capacity probe & high speed scope. Yes: ok No: Check bias on Q2, if ok replace Q1. |
| L.O. Signal | Is LO at base of Q34 about 1Vpp? Yes: Check collector for about 2Vpp. No: Check signal path back to LO input cable from Synthesizer. |

Readout

| | |
|---|---|
| 5 of any one segment always on (any degree of brightness) | Sixth digit--the one digit with segment <u>off</u> should be replaced. |
| Incorrect numbers displayed | Does movement of synth boards cause display to change?<br>Yes: Check for parts shorting between boards & clean contacts of connectors.<br>No: Most likely cause of fault is IC29 on synth #1, segment enable. |
| No Display | Are bright & dim voltages present?<br>Yes: Check inter-board connectors for digit enable & segment enable pulses. |

Synthesizer:

Frequency fails to lock:

Is Minor loop locked? This is determined by fixed correction voltage near 1.5VDC & fixed pulse pattern on IC9 pin 13.

Yes: Proceed to major loop.

No: Are data and reference present at pins 1 & 3 of IC9? These are narrow pulses and it may require a counter to determine their presence. The counter should read 165Hz.

If no data is present at pin 1 of IC9 check VCO clock output on pin 14 of IC16 and signal trace IC16 output (pin 11) through the divider chain IC's 15 through 11. IC10 is a oneshot MV that provides reset for the counters and data signal to IC9.

If no reference signal is present at IC9, pin 3 check the 5MHz clock signal at pin 1 of IC5. Signal trace divider signal through IC's 5, 4, 8, 7 and 6. IC10 provides a similar function to this divider as the data divider.

If data and reference signals are present; are pulses present at either pin 10 or pin 13 of IC9? If not replace IC9.

If pulses are present at either pin 10 or 13 is a slowly varying DC level present at pin 8 of IC9. If not replace IC9. If this signal is present trace it through the notch filter (IC20) and the loop filters to the VCO input.

Is the major loop locked? Yes: System is operational

No: Procede by signal tracing in a manner similar to the minor loop.

Check for data and reference present at pins 1 and 3 of IC19. The data rate is 100Hz.

The reference divider chain is composed of IC's 5 through 1.

If reference is normal check for VCO operation. If VCO is normal signal trace through synthesizer mixer and clock driver to determine that the 2 to 4MHz clock is present. If clock is present determine if 100Hz data is present at output of major loop divider.

Check IC19 in a manner similar to IC9.

Frequency fails to scan:

1. Does unit fail to scan on both fast and slow?

Yes: Is 11V present at tuning switches?

Yes: Signal trace control voltages to synth #1 board and to IC's 31 and 32. With tuning switch depressed, check IC32 pin 11 for clock. Signal trace through pin 6 for "down" and pin 3 for "up"

If clock is present at pins 3 or 6 trace signal through programming ripple counter, IC's 16 through 20.

No: Signal trace switch and tracks. Determine plated through holes are making through contact.